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(21)Application number : 05-007725 (71)Applicant : OLYMPUS OPTICAL CO LTD
(22)Date of filing : 20.01.1993 (72)Inventor : YAMADA HIDETOSHI

(54) SOLID STATE IMAGE PICKUP DEVICE

(57)Abstract:
PURPOSE: To provide the solid state image pickup device which can pick up an image in a short storage period by simple structureand start and end the storage of all pixels at the same timing.
CONSTITUTION: The solid state image pickup device consists of a pixel group formed by arranging pixels 10-11 to 10-mn composed of amplification type photodetecting elements in matrixplural row lines 11-1 to 11-m to which the gates of the pixels arranged in an X direction in the pixel group are connected in commonplural column lines 12-1 to 12-n to which the sources of the pixels arrayed in a Y direction in the pixel group are connected in commona storage part where storage cells (capacitor) 15-11 to 15-mn storing video signals of the respective pixels on the respective row lines are arranged in matrixa vertical scanning circuit 24 which applies a pixel read signal to the row lines in orderand a horizontal scanning circuit 25 which outputs a driving signal for outputting video signal currents stored in the respective storage cells in order.

CLAIMS

[Claim(s)]
[Claim 1]A solid state camera which is provided with the following and characterized for an electric charge of each row line of a pixel group

provided in an imaging device by a storage start and ending to the same timing in a storage area.
A pixel group which has arranged a pixel which consists of an amplified type photo detector to matrix form.
Two or more row lines which carry out common connection of the gate of each pixel arranged in the direction of X of said pixel group.
Two or more sequence lines which carry out common connection of the sauce of each pixel arranged in the direction of Y of said pixel group.
A storage parts store by which two or more storage cells which memorize a video signal of each pixel of each of said row line have been arranged at matrix forma vertical scanning circuit which impresses a pixel read signal to said each row line one by oneand a horizontal scanning circuit which outputs a driving signal to which video signal current memorized by said each storage cell is made to output one by one.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the solid state camera which changes an optical image into an electrical signal using semiconductor technology.
[0002]
[Description of the Prior Art]Generallythere are solid state camerassuch as Charge Modulation Device (the following CMD is called) using the amplified type photo detector which consists of semiconductor devices as a pixel.
[0003]The example of composition of the solid state camera which used this conventional CMD as a pixel is shown in drawing 9. This CMD arranges CMD1-111-12 which constitutes each pixel--1-mn to matrix formand impresses video voltage V_{DD} (>0) to each of that drain in common. the source terminal of the CMD group of each sequence which connected to row line 2-12-2--2-m in common the gate terminal of the CMD group of each line arranged in the direction of Xrespectivelyand was arranged in the direction of Y -- sequence line 3-13-2--3-n -- it connects in commonrespectively. Sequence line 3-13-2--3-n are connected common to the video line 5 via transistor 4-14-2 for sequence selection--4-nrespectively.
[0004]Said video line 5 is connected to the current-voltage conversion

type preamplifier 6 by which the imaginary earth of the input edge was carried outand the video signal of negative polarity is read to the outgoing end 7 of the preamplifier 6 by a time series.
[0005]Row line 2-12-2--2-m are connected to the vertical scanning circuit 8and signal $phi_{G1}phi_{G2}$--phi_{Gm} are impressedrespectively. Direct continuation of the gate terminal of transistor 4-14-2 for sequence selection--4-n is carried out to the horizontal scanning circuit 9and it is constituted so that signal $phi_{S1}phi_{S2}$--phi_{Sn} may be impressedrespectively. Each CMD is formed on the same board and V_{SUB} (<0) is impressed to the substrate.
[0006]Drawing 10 is a signal waveform diagram for explaining operation of the solid state camera of composition of having been shown in drawing 9. Row line 2-12-of this solid state camera 2--signal phi_{G1} impressed to 2-mphi_{G2}--phi_{Gn} consist of read-out gate voltage V_{RD}reset voltage V_{RS}overflow voltage $V_{OF}$and accumulation voltage V_{INT}.
[0007]And in a non selection lineit becomes accumulation voltage V_{INT} into overflow voltage V_{OF} and level image shelf-life t_H into horizontal blanking interval t_{BL} of a video signal. In.a selection rowit reads into level image shelf-life $t_H$and becomes reset voltage V_{RS} into gate voltage V_{RD} and horizontal blanking interval t_{BL} which follows it.
[0008]Transistor 4-14-2 for sequence selection--signal phi_{S1} impressed to the gate terminal of 4-nphi_{S2}--phi_{Sn}By sequence line 3-13-2--the signal for choosing 3-nit is set up so that the low may become transistor 4-14-2 for sequence selection--a pressure value [one / the high level / turns off 4-n and / a pressure value / the transistor for sequence selection].
[0009]In the solid state camera of the above compositionwhen signal phi_{G1} becomes read voltageCMD of the 1st line is chosenThensignal $phi_{S1}phi_{S2}$--when one [phi_{Sn}]1-111-12--the signal current from one to 1 n are read via a video line one by one. Signal $phi_{G1}phi_{G2}$--phi_{Gm} are made into read voltage one by oneat every timesignal $phi_{S1}phi_{S2}$--phi_{Sn} become oneand the signal of all the pixels is read one by one.
[0010]
[Problem(s) to be Solved by the Invention]Howeverin the conventional solid state camera mentioned abovesince read-out of a signal is performed by sequential scanningthe timing of a storage start and an end will differ for every pixel.
[0011]Although it is convenient that such timing differs for a use which picturizes an animation and is reproduced as it istrouble appears in usessuch as image measuringfor example. That isin order to measure the object which moves at high speedit is short exposure time and it is

necessary to acquire the picture of identical time butand in the conventional solid state camerasince the read time which became settled in order to acquire one picture is neededone perfect picture cannot be acquired by the short exposure time not more than it.
[0012]As a solid state camera which solves this faultthere is a solid state camera which transmits the electric charge accumulated for every pixel to an amplifier so that it may be proposed by JP61-84058A. Howeverin said solid state camerasince the structure of a pixel becomes complicated and area also becomes largethere is a fault that high integration is difficult.
[0013]Thenthis invention aims to let all the pixels provide the solid state camera in which a storage start and an end are possible to the timing that it can picturize in a short storage period with an easy structure.
[0014]
[Means for Solving the Problem]A pixel group which has arranged a pixel which consists of an amplified type photo detector to matrix form in order that this invention may attain the above-mentioned purposeTwo or more row lines which carry out common connection of the gate of each pixel arranged in the direction of X of said pixel groupTwo or more sequence lines which carry out common connection of the sauce of each pixel arranged in the direction of Y of said pixel groupA storage parts store by which two or more storage cells which memorize a video signal of each pixel of each of said row line have been arranged at matrix formA vertical scanning circuit which impresses a pixel read signal to said each row line one by oneIt comprises a horizontal scanning circuit which outputs a driving signal to which video signal current memorized by said each storage cell is made to output one by oneand a storage area is provided with a storage start and a solid state camera to end for an electric charge of each row line of a pixel group provided in an imaging device to the same timing.
[0015]
[Function]The storage start and end of the solid state camera of the above composition are done to the timing that each pixel is almost the sameby providing the storage area which accumulates the electric charge of each row line of a light sensing portion in an imaging deviceand transmitting the accumulated electric charge via a sequence line.
[0016]
[Example]Hereafterwith reference to drawingsthe example of this invention is described in detail.
[0017]The composition of the solid state camera as the 1st example by

this invention is shown and explained to drawing 1. CMD10-1110-12 which constitutes each pixel in this solid state camera--10-mn are arranged by matrix form. Video voltage V_{DD} (>0) is impressed to each drain of CMD in common. As for the gate terminal of the CMD group of each line arranged in the direction of Xthe source terminal of row line 11-111-2--the CMD group of each sequence which was connected to 11-m in commonrespectivelyand was arranged in the direction of Y is connected to sequence line 12-112-2--12-n in commonrespectively. Sequence line 12-112-2--12-n are connected to accumulation sequence line 14-114-2--14-n via transfer transistor 13-113-2--13-nrespectively.

[0018]Each accumulation sequence line 14-114-2--capacitor arranged by 14-n at matrix form 15-1115-12--15-mn are connected via cell selection transistor 16-1116-12--16-mnand the accumulating part is formed. The gate of cell selection transistor 16-1116-12--16-mn is connected to accumulation row line 17-117-2 and 17-m.

[0019]And the end of accumulation sequence line 14-114-2--14-nWhile being connected to the gate of sequence read transistor 18-118-2--18-nit is connected also to the drain of sequence read transistor 18-118-2--18-n via accumulation selection transistor 19-119-2--19-n. The drain of said sequence read transistor 18-118-2--18-n is further connected common to the video line 21 via sequence selection transistor 20-120-2--20-n. The video line 21 is connected to the current-voltage conversion type preamplifier 22 by which the imaginary earth of the input was carried outand a video signal is read to the outgoing end 23 of said preamplifier 22 by a time series.

[0020]Row line 11-111-2--11-m are connected to the vertical scanning circuit 24and signal $phi_{C1}phi_{C2}$--phi_{Cm} are impressedrespectively. Similarly accumulation row line 17-117-2 and 17-m are connected to the vertical scanning circuit 24and signal $phi_{C1}phi_{C2}$--phi_{Cm} are impressedrespectively. Signal phi_T is impressed to the gate of transfer transistor 13-113-2--13-nand signal phi_H is impressed to the gate of accumulation selection transistor 19-119-2--19-n.

[0021]And direct continuation of the gate terminal of sequence selection transistor 20-120-2--20-n is carried out to the horizontal scanning circuit 25and it is constituted so that signal $phi_{S1}phi_{S2}$--phi_{Sn} may be impressedrespectively. Furthermoreaccumulation sequence line 14-114-2--14-n are connected to reset transistor 26-126-2--the line grounded via 26-n. Signal phi_{RS} is impressed to the gate of reset transistor 26-126-2--26-n in common from the vertical scanning circuit 24. Nextexample operation is explained to drawing 2 for the signal waveform diagram of each point of the solid state camera of composition of having been shown

in drawing 1.
[0022]Hererow line 11-111-2--signal phi_{G1} impressed to 11-mphi_{G2}--phi_{Gm} consist of read-out gate voltage V_{RD}reset voltage V_{RS}overflow voltage $V_{OF}$and accumulation voltage V_{INT}. Usuallyit is accumulation voltage V_{INT} and the inside of horizontal blanking interval t_{HBL} of a video signal becomes overflow voltage V_{OF}. The inside of vertical-retrace-line period t_{VBL} reads for every selection rowtakes gate voltage $V_{RD}$and becomes reset voltage V_{RS} at all the line coincidence following on it.
[0023]Firstall the CMD(s) are reset because phi_G to 11-m becomes [all the row line 11-111-2--] reset voltage simultaneously. Thena row line signal becomes accumulation voltage $V_{INT}$and accumulation of a photoelectrical load is started. In the pixel into which light enteredan electron hole is accumulated under the gate of CMD among the generated electron-hole pairs. For this reasonthe potential under the gate of CMD rises according to light volume.
[0024]The signal of each pixel is read after predetermined storage time. Signal phi_T and phi_H are set to "Hi" and read voltage and phi_{G1} are first set to "Hi" for phi_{G1}. CMD10-1110-12--ten to 1 n are chosen by thisThe signal current according to the stored charge of each pixel arisesand capacitor 15-1115-12--15 to 1 n are charged via sequence line 12-112-2--12-n and accumulation sequence line 14-114-2--14-nrespectively.
[0025]At this timeaccumulation selection transistor 19-119-2--since one [19-n]current arises also in sequence read transistor 18-118-2--18-n. And when the current of CMD10-11 and the current of the sequence read transistor 18-1 become equalthe charge to the capacitor 15-11 stopsand the potential which gives current equal to a pixel signal is memorized.
[0026]Similarlythe signal of CMD10-1210-13--ten to 1 n is simultaneously accumulated in capacitor 15-1215-13--15 to 1 n. Thenread voltage and phi_{G2} are set to "Hi"and phi_{G2} is simultaneously accumulated for the signal of CMD10-2110-22--ten to 2 n in capacitor 15-2115-22--15 to 2 n by the same operation.
[0027]Hereafterwhile phi_{G3}-$phi_{G3}$$phi_{G4}$-$phi_{G4}$--$phi_{Gm}$-$phi_{Gm}$ are turned onthe pixel signal of the 3rd linethe 4th line--eye m line is transmitted to the capacitor of an accumulating part.
[0028]And after transmission is completedphi_H is turned off and a signal is read from an accumulating part one by one. phi_{G1} becomes one first and the gate of sequence read transistor 18-118-2--18-n is connected to capacitor 15-115-2--15-nrespectively. By signal phi_{S1} being set to "Hi" herecurrent equal to the signal current of the pixel 10-11 to the sequence read transistor 18-1 is absorbed. Via the video line 21this current is transformed into voltage by the preamplifier 22and serves as

a signal of the pixel 10-11. Thenthe signal current of the pixel 10-12 is absorbed by the sequence read transistor 18-2 by signal phi_{S2} being set to "Hi."

[0029]Hereaftersignal read-out of the 1st line is performed by $phi_{S3}phi_{S4}$--phi_{Sn} being set to "Hi." Thenthe 2nd line is chosen by phi_{C2} being set to "Hi"and the signal of pixel 10-2110-22--ten to 2 n is read one by one by $phi_{S1}phi_{S2}$--phi_{Sn} being set to "Hi." Hereafter$phi_{C3}phi_{C4}$--phi_{Cn} are turned onand the pixel signal of the 3rd linethe 4th line--eye m line is read one by one. At the last of read-out of each linethe reset transistor 26 serves as one by $phi_{RS}$and the capacitor of accumulation sequence line 14-114-2--the line that 14-n is made into earth potentials and chosen is reset.

[0030]As mentioned abovein the solid state camera of this inventionthe signal transmission to an accumulating part from the pixel CMD bundles up within a vertical blanking periodand is performed. Since the transmission period for every line can also be shortened very muchit can consider that the timing of the storage start and end which is each pixel is almost the sameandthereforea still picture can be picturized in a short storage period.

[0031]Nextthe composition of the solid state camera as the 2nd example by this invention is shown and explained to drawing 3. Herethe same reference mark is given to a member equivalent to the members forming shown in drawing 1 by the members forming of the 2nd exampleand the explanation is omitted. Pixel CMD10-1110-12 by which this solid state camera was arranged at matrix form--10-mnIt has sequence line 12-112-2 which connects the source terminal of row line 11-111-2 which connects the gate terminal of the CMD group of each line arranged in the direction of X--the CMD group of each sequence arranged in 11-m and the direction of Y--12-n. Such sequence line 12-112-2--12-n are connected to accumulation sequence line 14-114-2--14-n via transfer transistor 13-113-2--13-nrespectively.

[0032]And each accumulation sequence line 14-114-2--capacitor arranged by 14-n at matrix form 15-1115-12--15- Ln are connected via cell selection transistor 16-1116-12--16- Lnand the accumulating part is formed. The gate of cell selection transistor 16-1116-12--16- Ln is connected to accumulation row line 17-117-2--17-1. In this examplemore numbers 1 of lines of the accumulating part than the number m of lines of a picture element matrix are formed.

[0033]The end of said accumulation sequence line 14-114-2--14-nIt is connected to the gate of sequence read transistor 18-118-2--18-nand is connected also to the drain of sequence read transistor 18-118-2--18-n

via accumulation selection transistor 19-119-2--19-n. The drain of sequence read transistor 18-118-2--18-n is further connected common to the video line 21 via sequence selection transistor 20-120-2 and 20-n.
[0034]Nextthe video line 21 is connected to the current-voltage conversion type preamplifier 22 by which the imaginary earth of the input was carried outand a video signal is read to the outgoing end 23 of this preamplifier 22 by a time series.
[0035]Row line 11-111-2--11-m are connected to the vertical scanning circuit 24and signal $phi_{G1}phi_{G2}$--phi_{Gm} are impressedrespectively. Accumulation row line 17-117-2 and 17-1 are connected to the selector 27and signal $phi_{C1}phi_{C2}$--phi_{Cm} are impressed to selected m line in 1 linerespectively. Furthermorethe selector 27 is connected to vertical scanning circuit 24 and ROM(read-only memory) 28. Signal phi_T is impressed to the gate of said transfer transistor 13-113-2--13-nand signal phi_H is impressed to the gate of accumulation selection transistor 19-119-2--19-n. Direct continuation of the gate terminal of said sequence selection transistor 20-120-2--20-n is carried out to the horizontal scanning circuit 25and it is constituted so that signal $phi_{S1}phi_{S2}$--phi_{Sn} may be impressedrespectively. Furthermoreaccumulation sequence line 14-114-2--14-n are connected to reset transistor 26-126-2--the line grounded via 26-m.
[0036]The solid state camera of this 2nd example investigates the existence of the defect of an accumulating part in the stage where the solid state camera was manufacturedand there is in replacing with a spare accumulation line to a line with a defect. For this reasonit becomes usable also with the chip which has some defects in an accumulating part. In advance of operation of a solid state camerathe capacitor of an accumulating part and operation of a cell selection transistor are checked by a semiconductor circuit tester etc. When there is a malfunction by a crystal defect or leakthe line is recordedand it is replaced with a reserve line. This replacement information is recorded on ROM28 of a vertical scanning part.
[0037]After the above-mentioned information setting is madeoperation of this solid state camera is fundamentally the same as that of the 1st example. All the CMD(s) are reset because phi_G to 11-m becomes [all the row line 11-111-2--] reset voltage simultaneously. Thena row line signal becomes accumulation voltage $V_{INT}$and a photoelectrical load is accumulated. The signal of each pixel is read after predetermined storage time. Signal phi_T and phi_H are set to "Hi" and read voltage and phi_{Ci} are first set to "Hi" for phi_{Gi}. The 1st line of a picture element part is chosen by thisthe signal current according to the stored charge

which is each pixel arisesand the capacitor of an accumulation line (it was replacedwhen the 1st line did not have a defect and there were the 1st line and a defect line) applicable via a sequence line and an accumulation sequence line is charged. When the current of CMD and the current of a sequence read transistor become equal in each sequencethe charge to a capacitor is stopped and the potential which gives current equal to a pixel signal is memorized. Hereafterwhile phi_{G2}-$phi_{G2}$$phi_{G3}$-$phi_{G3}$--$phi_{Gm}$-$phi_{Gn}$ are turned onthe pixel signal of the 3rd linethe 4th line--eye m line is transmitted to the capacitor of an accumulating part. As mentioned abovewith the solid state camera of the 2nd examplealso with the chip which has some defects in an accumulating partit becomes usableand the yield improves and cost becomes cheap.

[0038]Nextthe composition of the solid state camera as the 3rd example by this invention is shown and explained to drawing 4. Herethe same reference mark is given to a member equivalent to the members forming shown in drawing 1 by the members forming of the 3rd exampleand the explanation is omitted.

[0039]Pixel CMD10-1110-12 by which this solid state camera was arranged at matrix form--10-mnIt has sequence line 12-112-2 which connects the source terminal of row line 11-111-2 which connects the gate terminal of the CMD group of each line arranged in the direction of X--the CMD group of each sequence arranged in 11-m and the direction of Y--12-n. Sequence line 12-112-2--12-n are connected to accumulation sequence line 14-114-2--14-n via transfer transistor 13-113-2--13-nrespectively.

[0040]Each accumulation sequence line 14-114-2--capacitor arranged by 14-n at matrix form 15-1115-12--15-mn are connected via cell selection transistor 16-1116-12--16-mnand the accumulating part is formed. The gate of cell selection transistor 16-1116-12--16-mn is connected to accumulation row line 17-117-2--17-m.

[0041]The end of said accumulation row line 14-114-2--14-nIt is connected to the gate of sequence read transistor 18-118-2--18-nand is connected also to the drain of sequence read transistor 18-118-2--18-n via accumulation selection transistor 19-119-2--19-n. The drain of said sequence read transistor 18-118-2--18-n is further connected common to the video line 21 via sequence selection transistor 20-120-2--20-n. This video line 21 is connected to the current-voltage conversion type preamplifier 22 by which the imaginary earth of the input was carried outand a video signal is read to the outgoing end 23 of the preamplifier 22 by a time series.

[0042]Row line 11-111-2--11-m are connected to the vertical scanning circuit 24and signal $phi_{G1}$$phi_{G2}$--$phi_{Gm}$ are impressedrespectively. Signal

$phi_{C1}$$phi_{C2}$--$phi_{Cm}$ are impressed to accumulation row line 17-117-2 and 17-1respectively. Signal phi_T is impressed to the gate of transfer transistor 13-113-2--13-nand signal phi_H is impressed to the gate of accumulation selection transistor 19-119-2--19-nrespectively. Direct continuation of the gate terminal of sequence selection transistor 20-120-2--20-n is carried out to the horizontal scanning circuit 25and it is constituted so that signal $phi_{S1}$$phi_{S2}$--$phi_{Sn}$ may be impressedrespectively. Furthermoreaccumulation sequence line 14-114-2--14-n are connected to reset transistor 26-126-2--the line grounded via 26-n.

[0043]Current store circuit 30-130-2--30-n are connected to said sequence line 12-112-2--12-n. Signal $phi_{R1}$$phi_{R2}$and phi_T are impressed to each current store circuit from the vertical scanning circuit 24. The composition of a current store circuit is shown in drawing 5 here.

[0044]In this current store circuitthe transistor 31 by which the drain was connected to the sequence line 12and the transistor 32 constitute a current mirror circuit. Interconnection of the gate of the transistor 31 and the transistor 32 is carried outand the capacitor 35 is connected via the transistor 34. The drain of said transistor 32 is connected to the drain of the P channel transistor 36 via the transistor 40.

[0045]The drain of said P channel transistor 36 is connected to the capacitor 38 via the transistor 37. The capacitor 38 is connected between the gate of the P channel transistor 36and sauce. Signal phi_{R1} is impressed to the gate of the transistor 37and signal phi_{R2} is impressed to the gate of the transistor 34.

[0046]The drain of said transistor 31 is connected to the drain of the transistor 36 via the transistor 39 at the gate of the transistor 31 via the transistor 33respectively. The inversion signal of phi_T with which signal phi_T is outputted to the gate of the transistor 33 and the transistor 40 from the inverter 41 again is impressed to the gate of said transistor 39respectively.

[0047]The solid state camera of this 3rd example records the information which deducted the output level at the time of the dark of each pixel from the signal level on an accumulating part. For this reasondispersion in the black level of each pixel can be canceledand the output with which the fixed pattern noise was reduced can be obtained. Nextwith reference to the signal waveform diagram of drawing 6operation of the solid state camera constituted in this way is explained.

[0048]Firstsignal transmission to an accumulating part from a picture element part is performed to vertical blanking period t_{VBL} like a last example. Impress-pulses phi_{G1} to the row line 11-1 turns into read

voltage V_{RD} at the time of a transfer startand signal phi_{R1} is simultaneously set to "Hi" at this time. For this reasonthe signal current read from each pixel of the 1st line is reversed in the current mirror circuit of the current store circuit 30current equal to the P channel transistor 36 arisesand the gate potential at this time is memorized by the capacitor 38. Thenphi_{G1} turns into reset voltage $V_{RS}$and the stored charge of each pixel is reset.

[0049]Furthermore phi_{G1} turns into read voltage V_{RD} againthe signal of the black level of each pixel is readand when phi_{R2} is turned onthe signal current of a black level arises to the transistor 31and this gate potential is memorized by the capacitor 35.

[0050]Next $phi_{G1}$$phi_{T}$and phi_{H} are set to "Hi"and signal transmission to an accumulating part from the current store circuit 30 is performed (phi_{G1} turns into accumulation voltage V_{INT} at this timeand the signal from a pixel is not read). The signal current at the time of ** of a pixel arises in the P channel transistor 36 of said current store circuit 30and the signal current at the time of dark arises to the transistor 31. The current equivalent to both difference arises in the read transistor 18 via the sequence line 12 and the accumulation sequence line 14and the gate potential which gives this current is memorized by the capacitor 15 of the 1st line of an accumulating part. Succeedinglythe above operation also receives without the 2nd line and 3rd line --and is performedand the pixel signal with which the black level was canceled is memorized by the accumulating part.

[0051]After thisthe potential memorized by the capacitor of the accumulating part is impressed to the gate of a read transistor one by one for every line like each example mentioned aboveand a signal is read via the video line 21 and the preamplifier 22.

[0052]In this 3rd examplethe information which deducted the output level at the time of the dark of each pixel from the signal level can be recorded on an accumulating partand the output with which dispersion in the black level of each pixel was canceledand the fixed pattern noise was reduced can be obtained.

[0053]Nextthe composition of the solid state camera of the 4th example by this invention is shown and explained to drawing 7. This example unifies functionally a solid state camera and the processing to the picturized picture.

[0054]Pixel CMD10-1110-12 by which this solid state camera was arranged at matrix form--10-mnIt has sequence line 12-112-2 which connects the source terminal of row line 11-111-2 which connects the gate terminal of the CMD group of each sequence arranged in the direction of X--the CMD

group of each sequence arranged in 11-m and the direction of Y--12-n. Sequence line 12-112-2--12-n are connected to accumulation sequence line 14-114-2--14-nrespectively. Each accumulation sequence line 14-114-2--14-n and accumulation row line 17-117-2--process element arranged by 17-m at matrix form 42-1142-12--42-mn are connectedand the storing processing part is formed.

[0055]The composition of a process element is shown in drawing 8 here. In this process elementthe input from the accumulation sequence line 14 is memorized via the selection transistor 16 in the signal hold circuit 44. The gate of said selection transistor 16 is connected to the accumulation row line 17and the signal hold circuit 44 is connected to the processor 46 via the quantization circuit 45.

[0056]Operation of the process element constituted in this way is explained. The signal charge accumulated by each pixel is transmitted to an accumulating part one by one for every line from a light sensing portion. That isthe current of the pixel CMD is current in the signal hold circuit 44 of a process element with the selected selection transistor 16. - Voltage conversion is carried out and potential is held at a capacitor. This signal is changed into digital valuessuch as binary-izing or 2 bitsand 4 bitsin the quantization circuit 45. The digitized signal is inputted into the processor 46 and it processes using the signal from the quantization circuit 45and the signal transmitted from a nearby processor in the processor 46.

[0057]As processing herethere are edge extractionthinningmoving object detectionlocus drawingetc. and it performs by the instruction given from a control circuit. A processing result is outputted in parallel from each processor.

[0058]the picture of the object which the processing to this solid state camera and a picture is unified functionallyfor exampleis suitable for the solid state camera of the 4th example for usessuch as image measuringas mentioned aboveand moves at high speed — all the **** -- it is possible to picturize to the almost same timing and to perform processing for measurement. as explained abovethe solid state camera of this invention can perform the image pick-up in a short storage period with an easy structure -- and all the **** -- a storage start and closing can be performed to the almost same timing. As for this inventionit is needless to say for the modification and application various in the range which are not limited to the example mentioned above and do not deviate from the gist of an invention to others to be possible.

[0059]

[Effect of the Invention]As explained in full detail aboveaccording to this inventionthe solid state camera [in the timing] which all the pixels can end [a storage start and] can be provided that it can picturize in a short storage period with an easy structure.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the composition of the solid state camera as the 1st example by this invention.
[Drawing 2]It is a signal waveform diagram of each point of the solid state camera of composition of having been shown in drawing 1.
[Drawing 3]It is a figure showing the composition of the solid state camera as the 2nd example by this invention.
[Drawing 4]It is a figure showing the composition of the solid state camera as the 3rd example by this invention.
[Drawing 5]It is a figure showing the composition of the current store circuit of the solid state camera of the 3rd example.
[Drawing 6]It is a signal waveform diagram for explaining operation of the solid state camera of the 3rd example.
[Drawing 7]It is a figure showing the composition of the solid state camera as the 4th example by this invention.
[Drawing 8]It is a figure showing the composition of the process element of the solid state camera of the 4th example.
[Drawing 9]Drawing 9 is a figure showing the example of composition of the solid state camera by the conventional CMD.
[Drawing 10]Drawing 10 is a signal waveform diagram for explaining operation of the solid state camera of composition of having been shown in drawing 9.
[Description of Notations]
10-11 - 10-mn--Charge Modulation Device (CMD)11-1 - 11-m -- A row line12-1 - 12-n -- A sequence line13-1 - 13-n -- Transfer transistor14-1 - 14-n -- An accumulation sequence line15-11 - 15-mn -- Capacitor16-11 - 16-mn -- A cell selection transistor17-1 - 17-m -- Accumulation row line18-1 - 18-n [-- A video line22 / -- A preamplifier23 / -- An outgoing end24 / -- A vertical scanning circuit26-1 - 26-n / -- Reset transistor.] -- A sequence read transistor19-1 - 19-n -- An accumulation selection transistor20-1 - 20-n -- A sequence selection transistor21